



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
[www.uspto.gov](http://www.uspto.gov)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/766,212	01/29/2004	Masaru Takaishi	AI 325	3347
7590	03/06/2006		EXAMINER	
RABIN & BERDO, P.C. 1101 14 Street, N.W., Suite 500 Washington, DC 20005				TOLEDO, FERNANDO L
			ART UNIT	PAPER NUMBER
			2823	

DATE MAILED: 03/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)	
	10/766,212	TAKAISHI, MASARU	
	Examiner Fernando Toledo	Art Unit 2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### **Status**

1) Responsive to communication(s) filed on 14 December 2005.  
 2a) This action is **FINAL**.      2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### **Disposition of Claims**

4) Claim(s) 1-7 and 9 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 1-7 and 9 is/are rejected.  
 7) Claim(s) \_\_\_\_\_ is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### **Application Papers**

9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### **Priority under 35 U.S.C. § 119**

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### **Attachment(s)**

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.	4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s)/Mail Date. _____. 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) 6) <input type="checkbox"/> Other: _____.
--	--

## DETAILED ACTION

### *Response to Amendment*

### ***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu et al. (U. S. Patent 6,143,645 A) in combination with Hirao et al. US 5621247.

In re claim 1, Hsu, in the U. S. Patent 6, 143,645 A; figures 1-3 and related text, discloses

forming a silicon-containing thin film 500 in a region having a predetermined area including the inner surface of the contact hole on the surface of the semiconductor substrate;

forming an aluminum-containing thin film 520 on the surface of the semiconductor substrate on which the silicon-containing thin film is formed; and heating the semiconductor substrate on which the aluminum-containing thin film is formed to such a temperature as to cause silicon to diffuse with respect to aluminum (Column 4, Lines 15 - 30 and Figure 3).

*Wherein the semiconductor substrate is provided with a plurality of cells each including the contact hole, and*

*the ratio of the amount of silicon contained in the silicon-containing thin film formed in the region having the predetermined area per unit cell to the amount of aluminum supplied to a unit cell in the step of forming the aluminum thin film is not less than 0.1 % and not more than 2% by atomic ration.*

The present application discloses a new metallization technology in which a melting-point depressant is locally introduced into the metal layer where it contacts the sidewalls of contact/via holes. This is preferably accomplished by a thin wetting layer which is only exposed on the sidewalls of contact/via holes. The wetting layer lowers the melting point and yield stress of the primary metallization layer at the points where this will most help the primary metallization layer to fill the contact/via hole. Since the concentration of the melting-point depressant is localized near contact/via holes, problems of precipitation or etch residues are minimized. This is particularly advantageous with aluminum metallization, but is also applicable to other metallization systems, col. 2, lines 26-39.

One constraint on aluminum metallization is imposed by the phenomenon of junction spiking. When pure aluminum is heated (even below its melting point) it can dissolve silicon which is in contact with it. Thus if pure aluminum meets monocrystalline silicon at a contact hole, the aluminum may grow dendritically into the silicon during thermal cycling. Such aluminum growths can penetrate junctions in the silicon, and thus destroy the desired electronic device. The conventional solution to this problem is to use aluminum metallization which is alloyed with a small fraction of silicon, e.g. 1% atomic, col. 1, line 59 – col. 2, line2.

Thus typical aluminum alloys use silicon (typically one half percent to 1% atomic) col. 2, lines 17-18.

The excess silicon or germanium in the liner will diffuse into the aluminum alloy, lower the melting point of the aluminum alloy, and lower the yield stress, and increase the lateral diffusivity of aluminum. The lower aluminum melting point enables faster aluminum transport at lower temperatures, and thus a lower temperature is adequate for complete filling. The arrows in FIG. 3 show approximate diffusion gradients during this diffusion, col. 3, lines 46-52.

Although Hsu's fig. 3 shows one cell and Hsu's col. 2, lines 26-39 above shows a plurality of cells represented by "contact/via holes" in plural form; the reference does not make very clear the cell as in a memory cell which including a contact hole.

The Hirao et al. reference teaches

The MOS transistors in the above cell select/drive circuit region 50 can be divided into two types depending on their functions: some of them serve as select transistors, while the others serve as drive transistors. The drain of the select transistor is in contact with a first plug 56 filled in a contact hole formed in the insulating layer 55, while the upper end of the plug 56 is in contact with the lower end of the first aluminum interconnection 52 in the memory cell region 60. The source of the select transistor is in contact with a bit line 57 indicated by the broken line in the drawing at a portion not shown in the cross section of FIG. 9. A word line extends in the direction orthogonal to the cross section of FIG. 9 over the isolation 52 and active region, while functioning as the gate electrode 53 in the individual active region. On the other hand, the source of the leftmost drive transistor in FIG. 9 is in contact with the second aluminum interconnection 66 of the memory cell region 60, while the drain thereof is in contact with a power-source terminal via the corresponding second plug 58, col. 13, lines 49-67.

It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the multiple cells of Hirao et al. with the method of making aluminum-containing thin film for contact holes of Hsu et al. because the method of Hsu et al. would provide the contact of Hirao et al. with reduced temperature contact/via filling as taught by Hsu et al. (col. 2).

3. In re claim 2, Hsu discloses wherein the step of forming an aluminum-containing thin film and the step of heating the semiconductor substrate is carried out simultaneously.

In this class of embodiments, step 110 is followed by step 120B. In this step aluminum alloy is reflowed into the cavity 202 by one step sputtering at elevated temperatures (e.g. greater than or equal to 350 degrees C. but preferably less than 450 degrees C.) and low power (to allow time for the aluminum to diffuse into the contacts and vias), col. 4, lines 14-19.

4. In re claim 3, Hsu discloses wherein the step of heating the semiconductor substrate is carried out after completing the step of forming an aluminum-containing thin film.

Alternatively a multistep sputtering operation can be used, first at low temperature (e.g. less than 100 degrees C.), then at high temperature (e.g. greater than 400 degrees C.). In either case the wetting layer introduces an addition of a melting-point depressant which will diffuse into the aluminum for a short distance to locally lower its melting point, and thus increase the diffusivity of aluminum along the surface. (The tendency of dopants to segregate to the surface is very advantageous in this regard.) Therefore, complete filling by aluminum reflow at lower temperatures can be obtained. FIG. 2C2 shows an intermediate step in this process, and FIG. 3 again shows the end result, col. 4, lines 19-31.

5. In re claim 4, Hsu discloses wherein the step of forming a silicon-containing thin film in the region having the predetermined area includes the step of: forming a silicon-containing thin film in a region larger than the predetermined area; and removing the silicon-containing thin film so that the area of the silicon-containing thin film can become the abovementioned predetermined area (Column 7, Lines 16 - 19).

6. In re claim 5, Hsu discloses wherein the step of removing the silicon-containing thin film includes a step of removing the silicon-containing thin film using a mask having a predetermined pattern (it is conventional in the art that to form a plug a mask must be used to avoid etching the plug).

7. In re claim 6, Hsu discloses wherein the step of removing the silicon-containing thin film includes a step of removing the silicon-containing thin film by etching (it is well-known in the art and conventional to remove unwanted portions by etching).

8. In re claim 7, Hsu discloses wherein the predetermined area is not more than 99% of the area of the aluminum-containing thin film formed in the step of forming the aluminum thin film (Figure 2).

9. In re claim 9, Hsu discloses wherein the step of heating the semiconductor substrate includes a step of heating the semiconductor substrate to 380 °C – 570 °C (Column 4, Lines 15-30).

### ***Response to Arguments***

10. Applicant's arguments filed 12/14/2005 have been fully considered but they are not persuasive.

11. Applicant argues, Remark's page 10, that Hsu et al. does "not disclose that the substrate 200 is heated". The examiner does not agree. Hsu's col. 4, lines 14-31 as quoted in the above rejection clearly teaches instant claim 2 "wherein the step of forming an aluminum-containing thin film and the step of heating the semiconductor substrate are carried out simultaneously" with aluminum alloy being reflowed into the cavity 202 by one step. Hsu et al. also teaches alternative operation of instant claim 3 "wherein the step of heating the semiconductor substrate is carried out after completing the step of forming the aluminum thin film" in which "multistep sputtering operation can be used, first at low temperature (e.g. less than 100 degrees C.), then at high temperature (e.g. greater than 400 degrees C.)". The sputtering operation of Hsu et al. is/are performed "at elevated temperature" "less than 450 °C" or "greater than 400 °C" in which the substrate 200 must be heated. Further, in the previous passage, Hsu et al.

teaches "filling was performed with high pressure extrusion of aluminum alloy at a heater temperature of 450 degrees C. (wafer temperature of 370 degrees C.), Hsu et al.'s col. 4, lines 4-6".

12. Applicant states, Remark's pages 11-12, "the only disclosure from this reference of atomic ratios is discussed in col. 2, lines 1-24 where the prior art configurations are discussed" and "it is impermissible to combine the teachings from the prior art disclosure discussed in the background of the invention of the cited reference with the disclosure directed to the embodiments discussed in the detailed description of the invention, as the examiner is apparently doing". The examiner does not agree. The previous rejection is under 35 U.S.C. 102(b) as being anticipated by Hsu et al. There is no combination because the Hsu et al.'s recognized ratio atomic percent in prior art (wherein a wetting layer is not used imposing spiking, precipitation and electromigration, col. 1, line 59 – col. 2, line 24) is used in Hsu et al.'s "new metallization technology" wherein "the wetting layer lowers the melting point and yield stress of the primary metallization layer at the points where this will most help the primary metallization layer to fill the contact/via hole", col. 2, lines 25-39. That recognized ratio atomic percent in prior art, used in Hsu et al., is inside the range of the claimed ratio.

13. Applicant's arguments with respect to claim 1 on the plurality of cells have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.
15. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh V. Pham whose telephone number is 571-272-1866. The examiner can normally be reached on M-Th (6:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2823

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TvP  
02/28/2006

*Matthew Smith*

MATTHEW SMITH  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2800